

**MS7043 Revision 1**  
**CHIPSET PT880+8237**

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**CPU:**

**Intel Northwood/Prescott**

**System Chipset:**

**PT880/PT800/P4X533 (North Bridge)**  
**VIA 8237/8235 (South Bridge)**

**On Board Chipset:**

**BIOS -- ISA EEPROM**  
**AC'97 Codec --VT1617**  
**LPC Super I/O -- W83697HF**  
**LAN -- VT6103L /VT6122**  
**CLOCK --ICS 952911A + ICS 93733**

**Main Memory:**


**DDR \* 2+1 (Max 3GB)**

**Expansion Slots:**

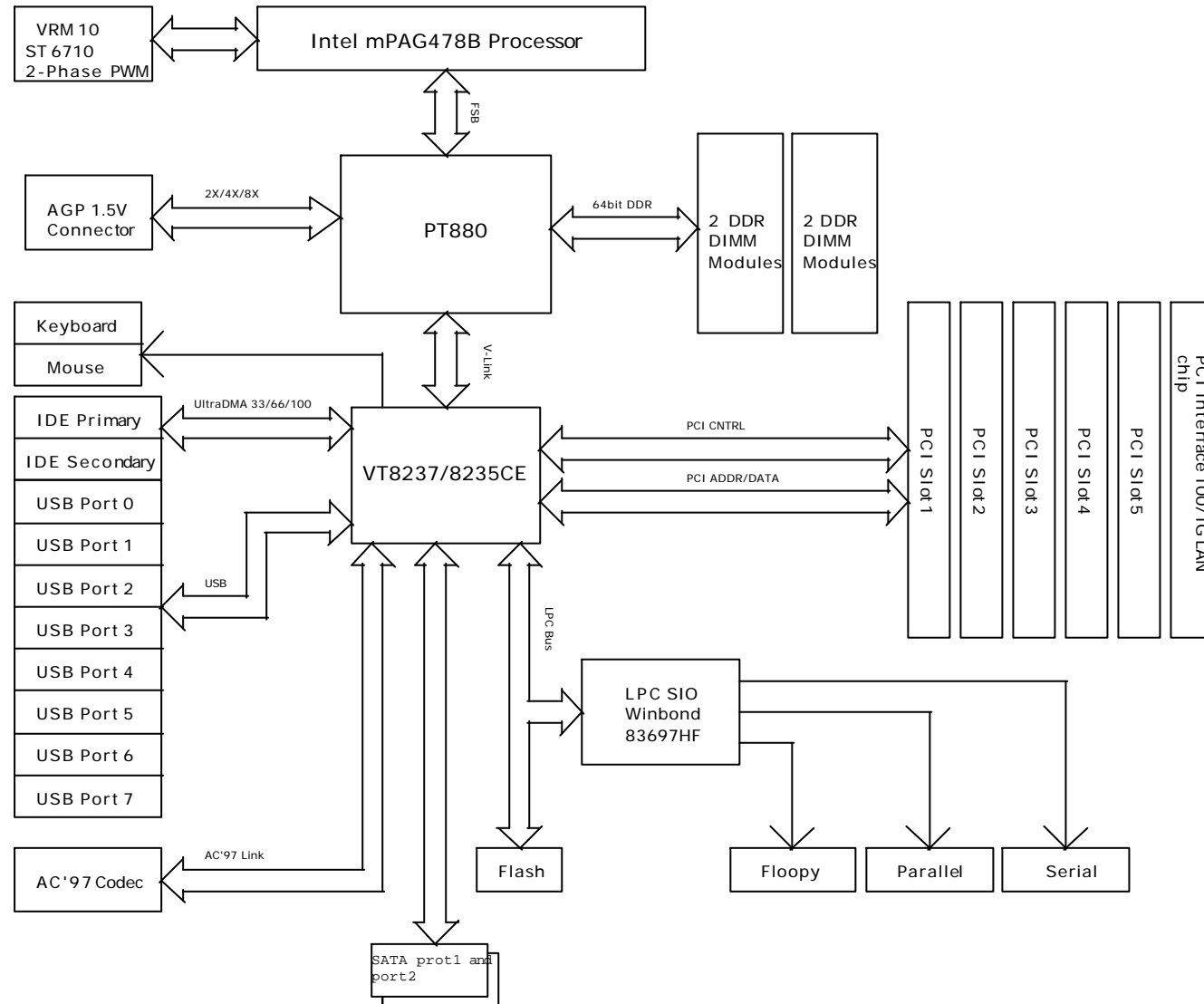
**PCI2.3 SLOT \* 5**

**PWM:**

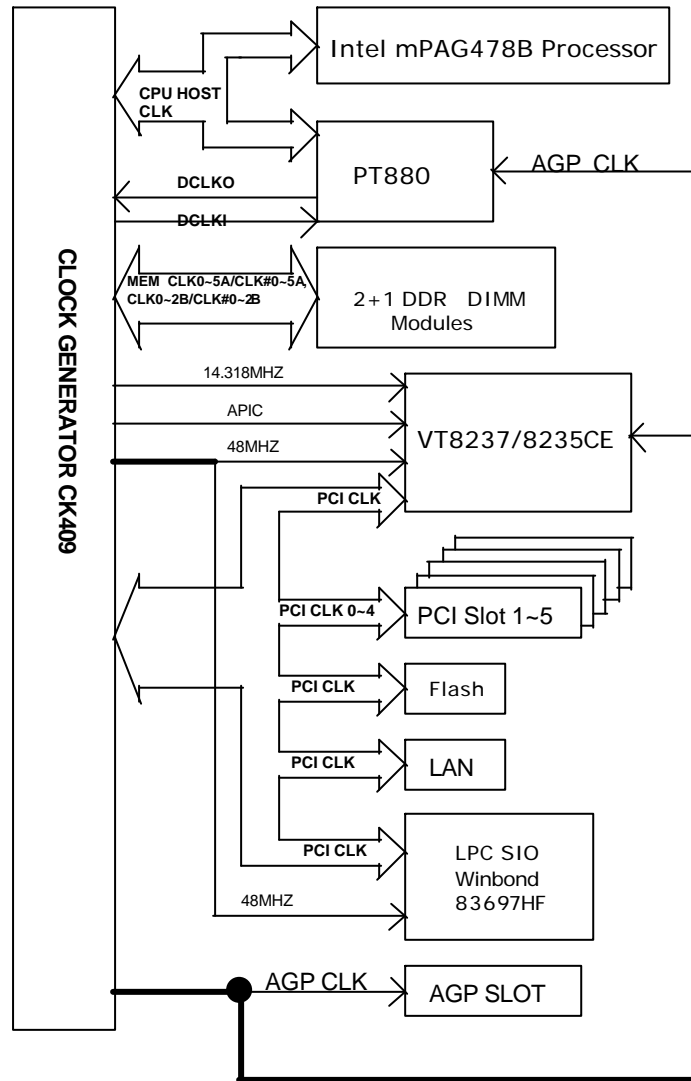
**Controller: ST 6710 /ST6709**

 <b>MICRO-STAR INT'L CO., LTD.</b>	
Title: COVER SHEET	
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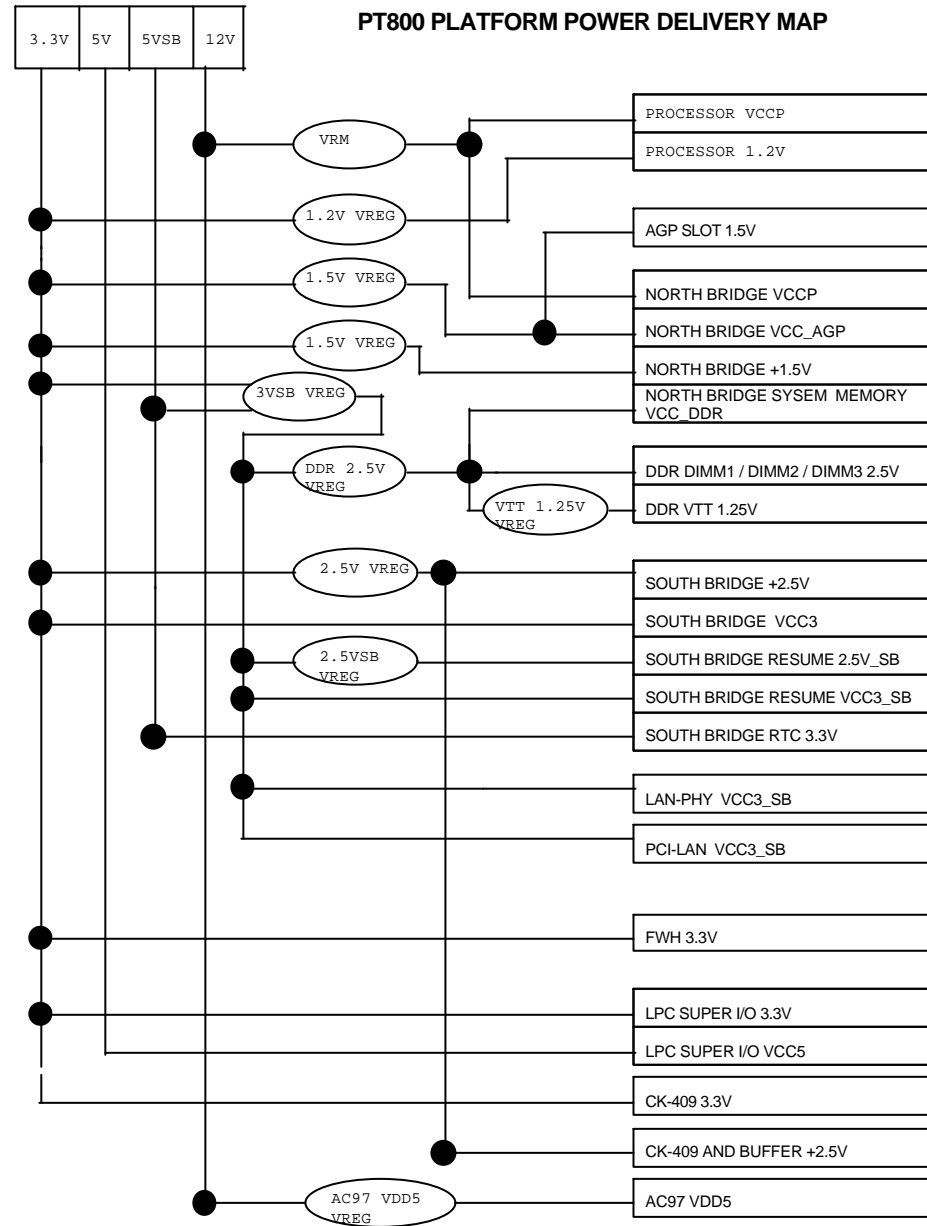
# Block Diagram



PT800 PLATFORM CLOCK GENERATOR MAP



PT800 PLATFORM POWER DELIVERY MAP



## NB

GPI O Pin	Type	Function	Power well
GPI 0	I	GPI 0	RESUME
GPI 1	I	IDE2 CBD	RESUME
GPO 0	I	GPO 0	RESUME
GPO 1	I	GPO 0	RESUME
GPIOA	I	NB STR S	MAIN
GPIOB	I	IOQDEPH	MAIN
GPIOC	I	NB STR S	MAIN
GPIOD	I	GTL PULL	MAIN

## I/O

GPI O 10	I/O	HI	MAIN
GPI O 11	I/O	HI	MAIN
GPI O 12	I/O	HI	MAIN
GPI O 13	I/O	NA	MAIN
GPI O 14	I/O	NA	MAIN
GPI O 15	I/O	NA	MAIN
GPI O 16	I/O	NA	MAIN
GPI O 17	I/O	NA	MAIN
GPI O 18	I/O	NA	MAIN
GPI O 19	I/O	NA	MAIN
GPI O 20	I/O	NA	MAIN
GPI O 21	I/O	NA	MAIN
GPI O 22	I/O	NA	MAIN

default output  
default output  
default output

## PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	PCI_REQ#0 PCI_GNT#0	AD19	PCICLK0	18 (PCI_CLK0)
PCI Slot 2	INTB# INTC# INTD# INTA#	PCI_REQ#1 PCI_GNT#1	AD20	PCICLK1	19 (PCI_CLK1)
PCI Slot 3	INTC# INTD# INTA# INTB#	PCI_REQ#2 PCI_GNT#2	AD21	PCICLK2	21 (PCI_CLK2)
PCI Slot 4	INTD# INTA# INTB# INTC#	PCI_REQ#3 PCI_GNT#3	AD22	PCICLK3	14 (PCI_CLK3)
PCI Slot 5	INTA# INTB# INTC# INTD#	PCI_REQ#4 PCI_GNT#4	AD23	PCICLK4	17 (PCI_CLK4)

## DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	MDCLKA0/MDCLKA#0 MDCLKA1/MDCLKA#1 MDCLKA2/MDCLKA#2
DIMM 2	1010001B	MDCLKA3/MDCLKA#3 MDCLKA4/MDCLKA#4 MDCLKA5/MDCLKA#5
DIMM 3	1010010B	MDCLKB0/MDCLKB#0 MDCLKB1/MDCLKB#1 MDCLKB2/MDCLKB#2

## FWH

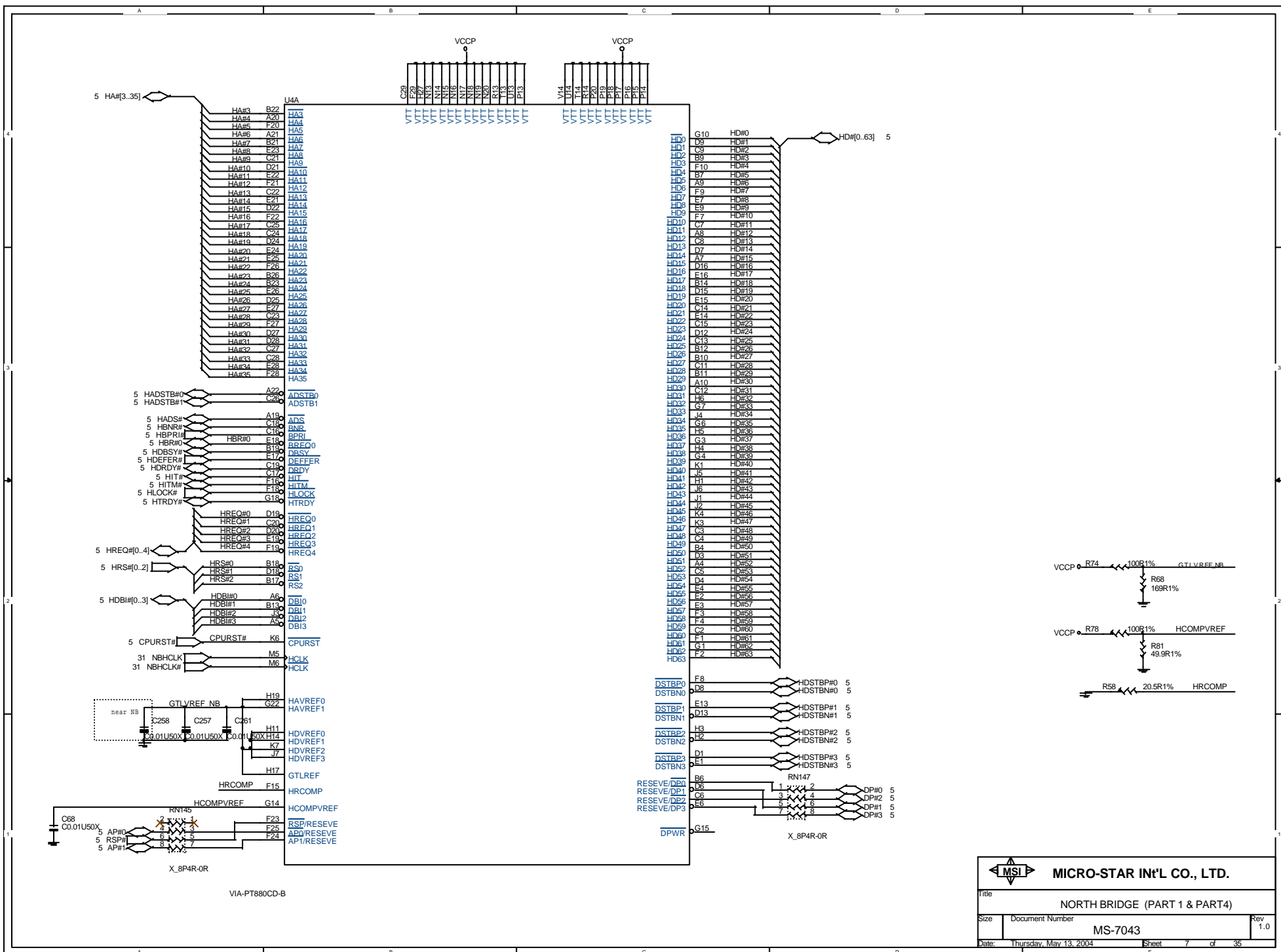
GPI O Pin	Type	Function
GPI 0	I	Pull UP through 1K ohms (unused)
GPI 1	I	Pull UP through 1K ohms (unused)
GPI 2	I	Pull UP through 1K ohms (unused)
GPI 3	I	Pull UP through 1K ohms (unused)
GPI 4	I	Pull UP through 1K ohms (unused)

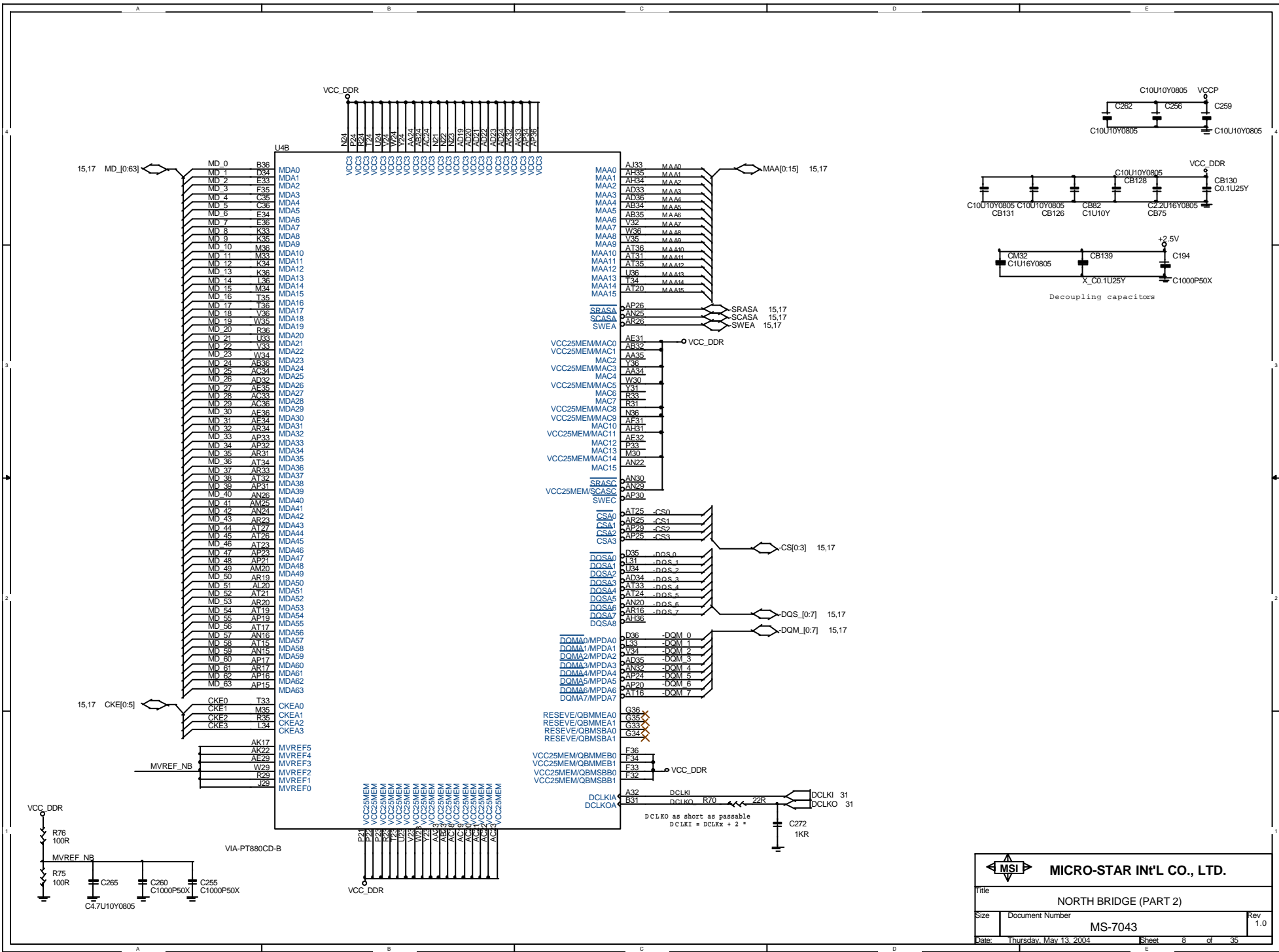
## PCI RESET DEVICE

Signals	Target
PCIRST#1	SB, NB
PCIRST#2	PCI slot 1-5, LAN,
HD_RST#	Primary, Scndary IDE

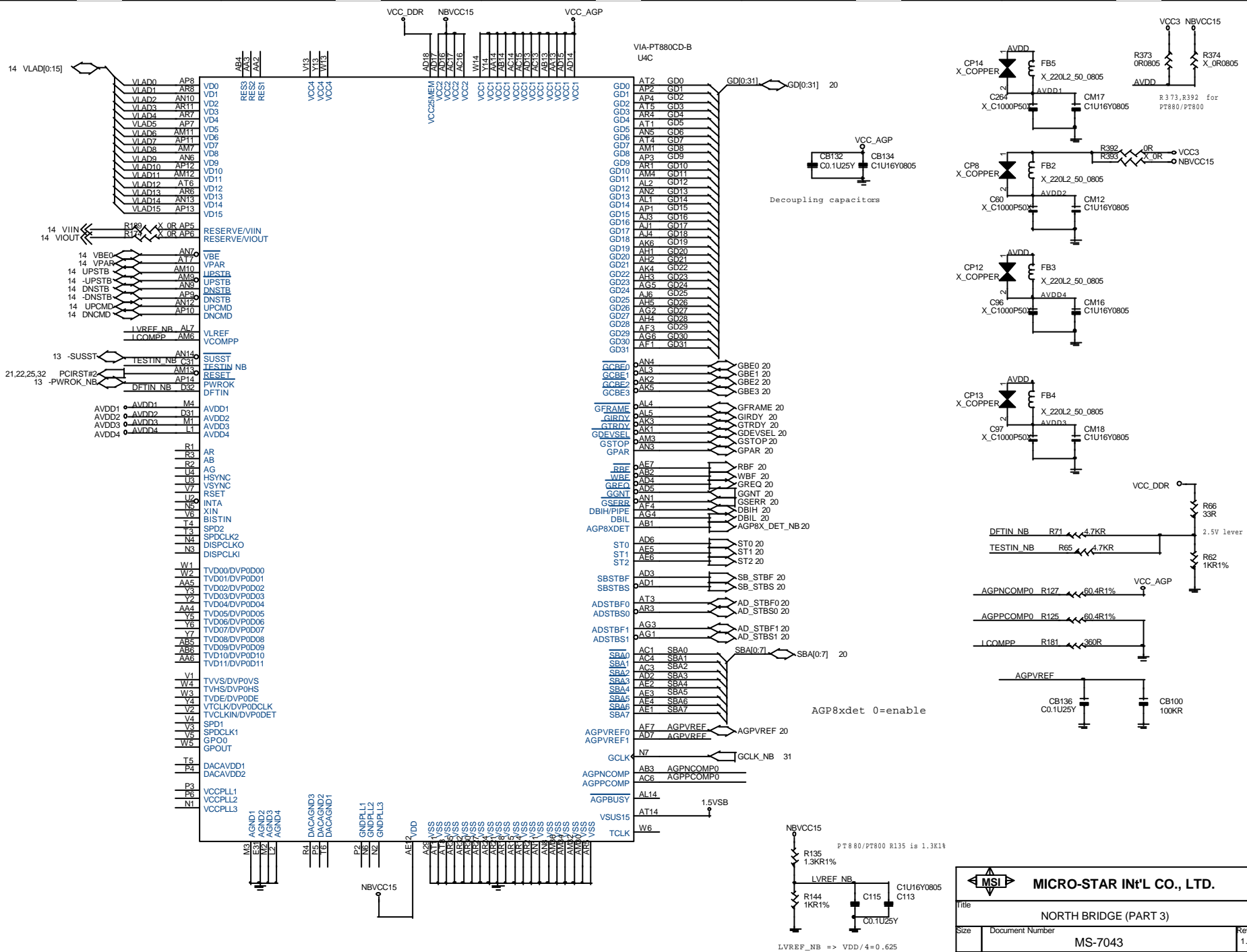


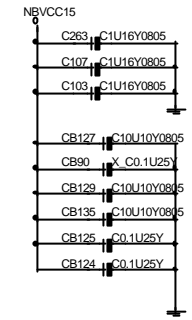
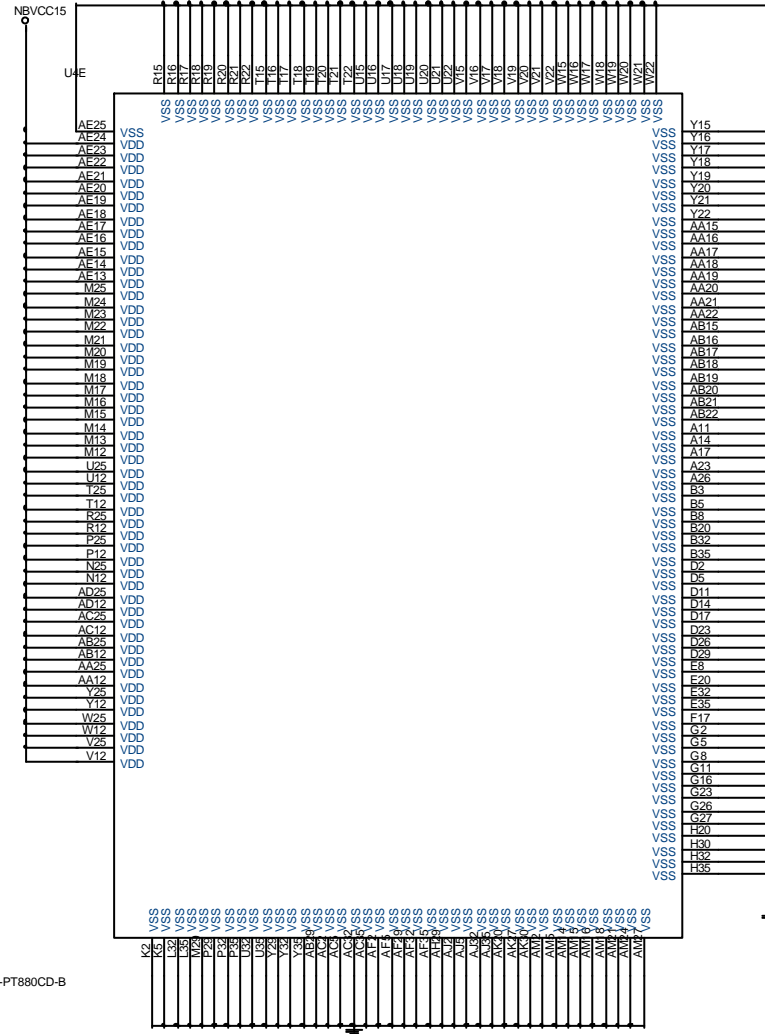


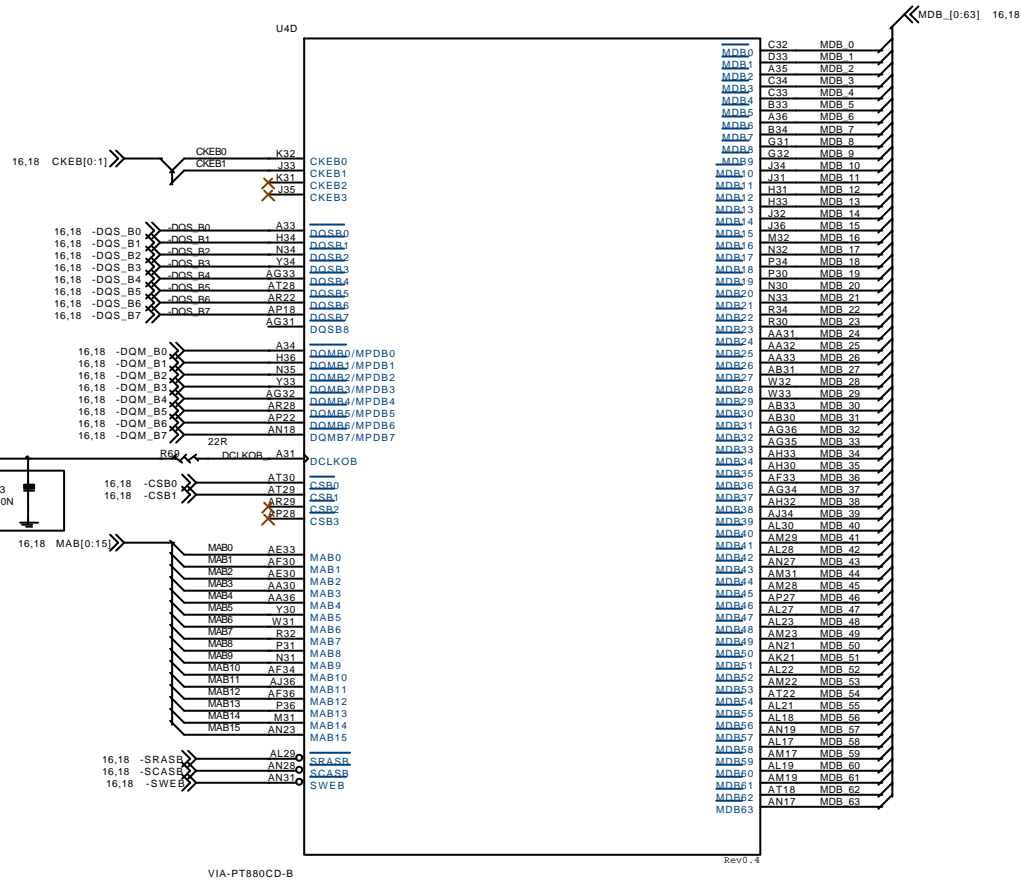


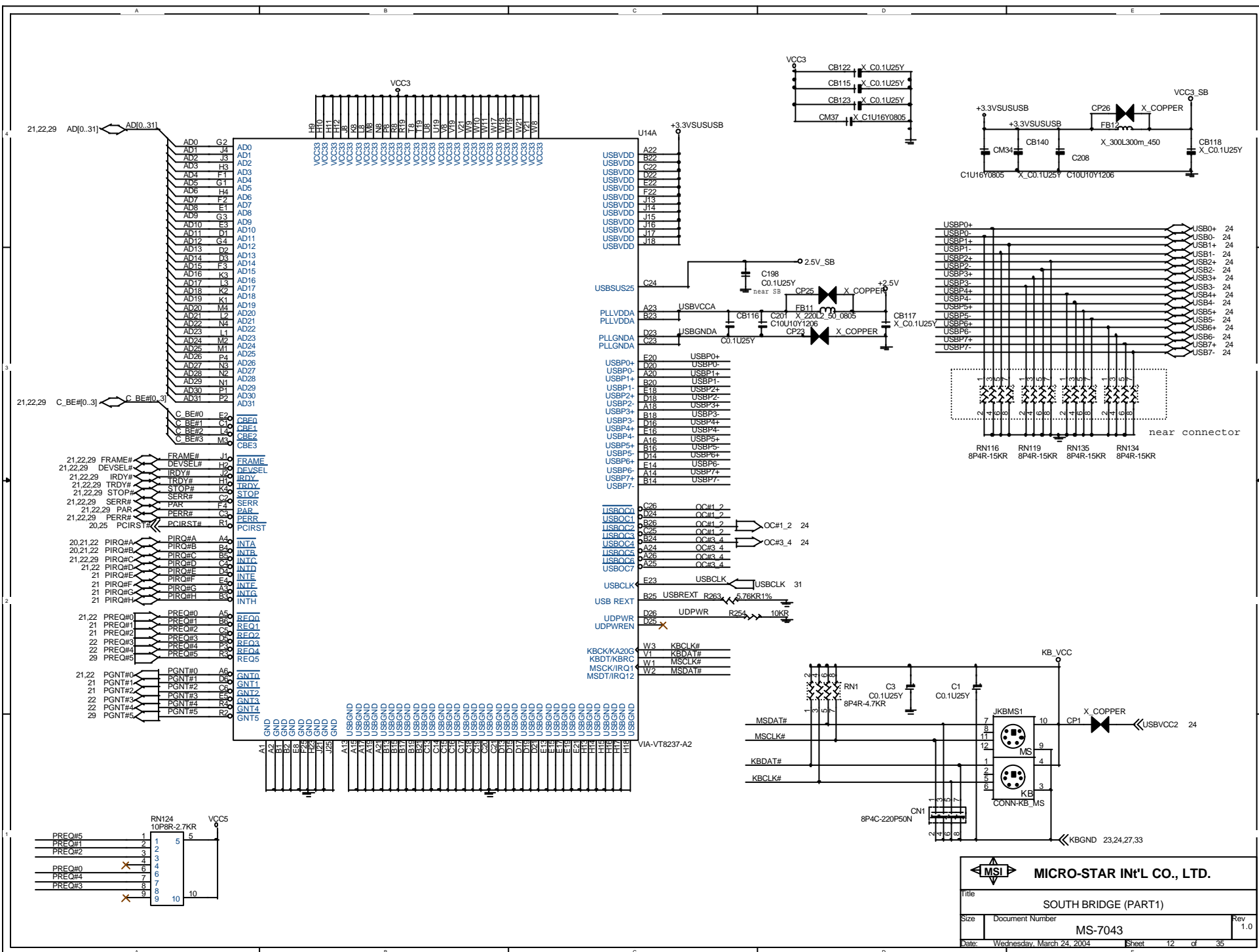


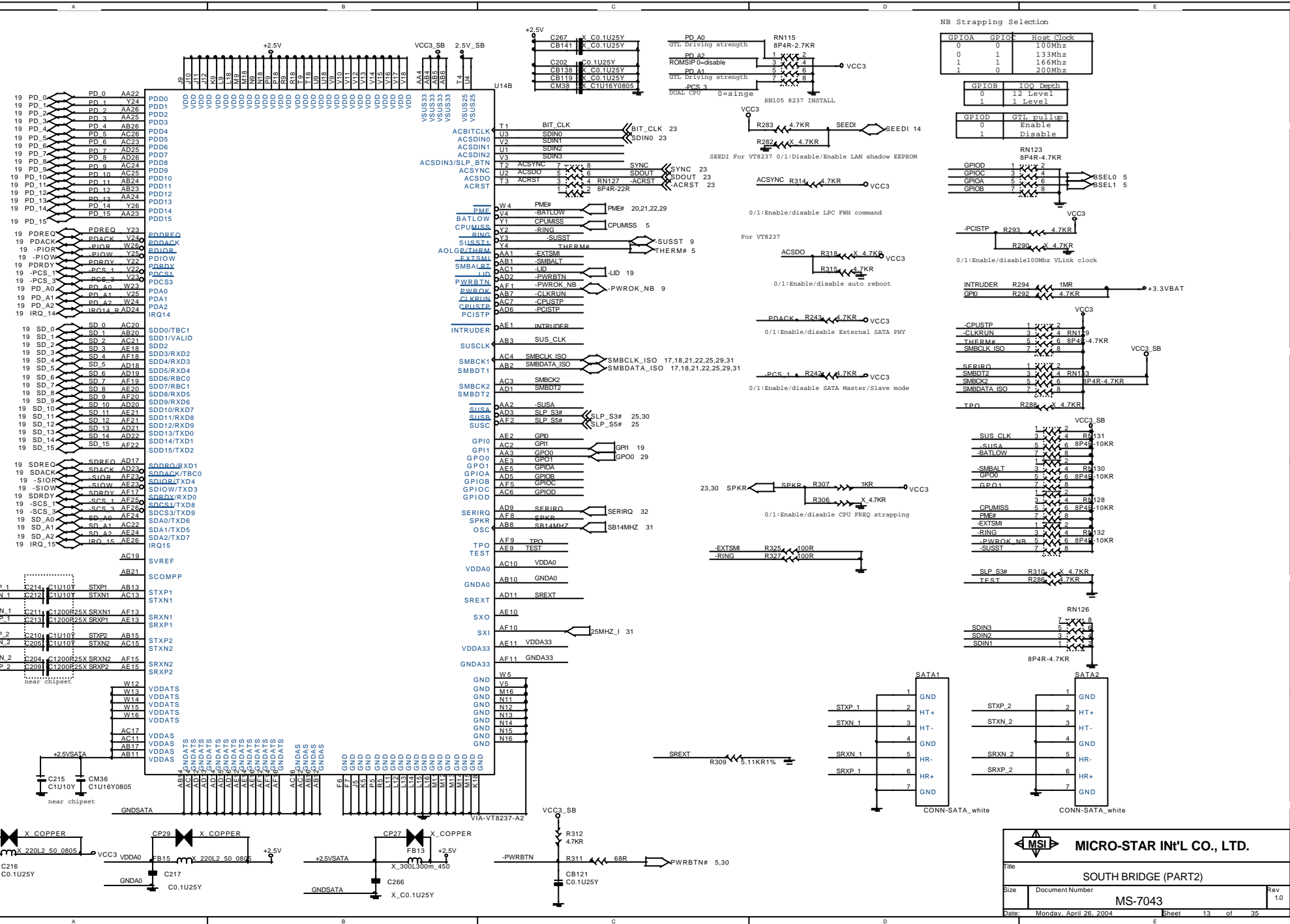










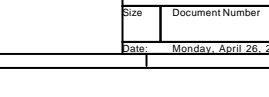
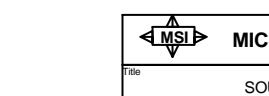
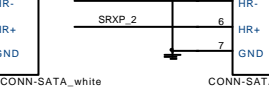
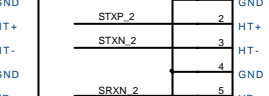
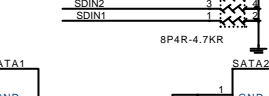
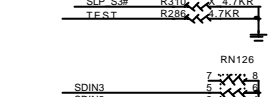
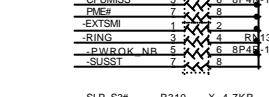
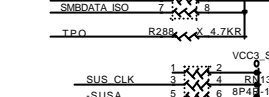
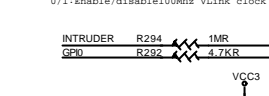
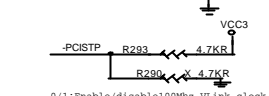
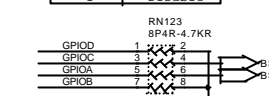



NB Strapping Selection

GPIOA	GPIOB	Host Clock
0	0	100Mhz
0	1	133Mhz
1	1	166Mhz
1	0	200Mhz

GPIOD	IOO Depth
0	12 Level
1	1 Level

GPIOD	GPIO Pullup
0	Enable
1	Disable



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File

SOUTH BRIDGE (PART2)

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Document Number

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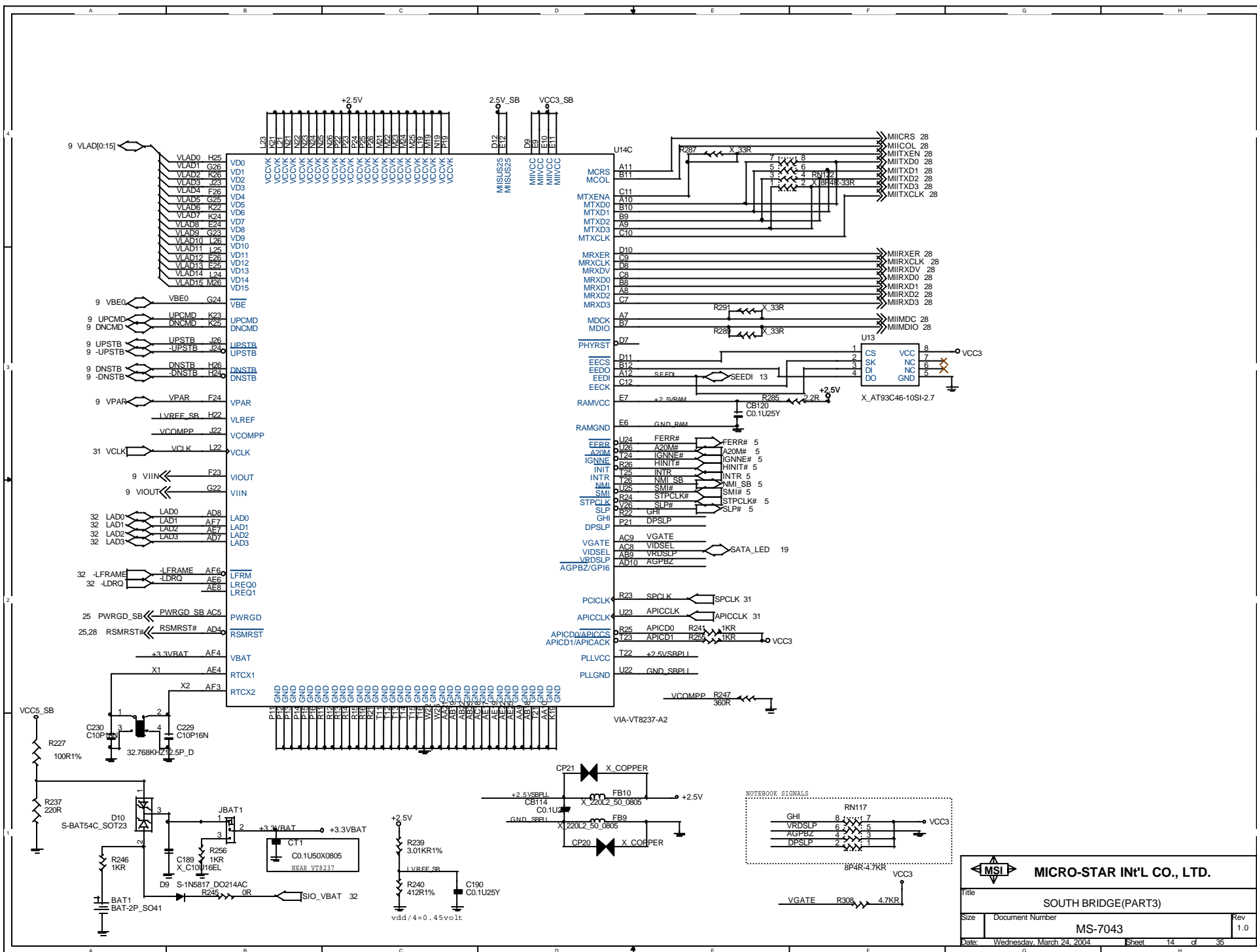
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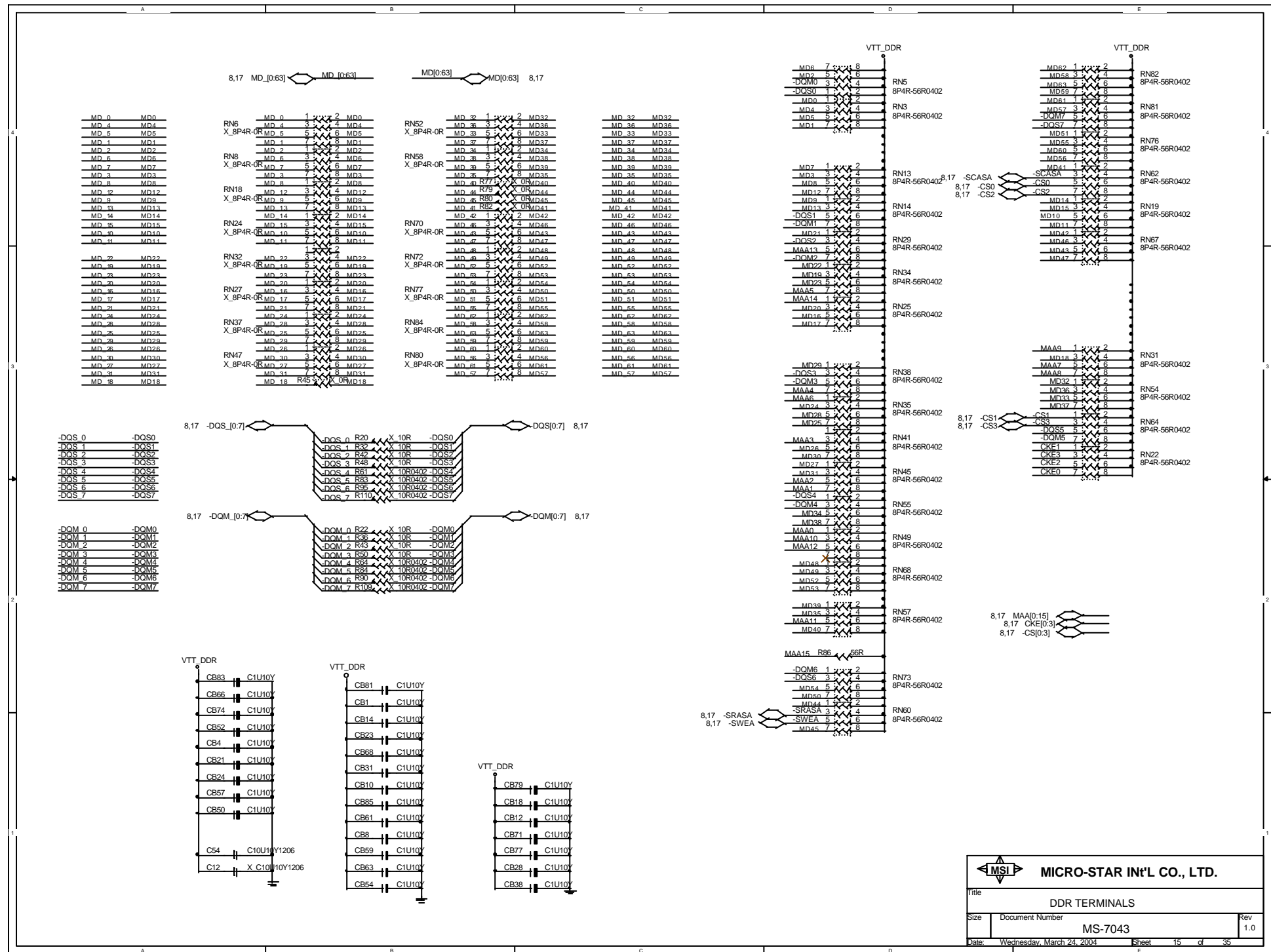
Date

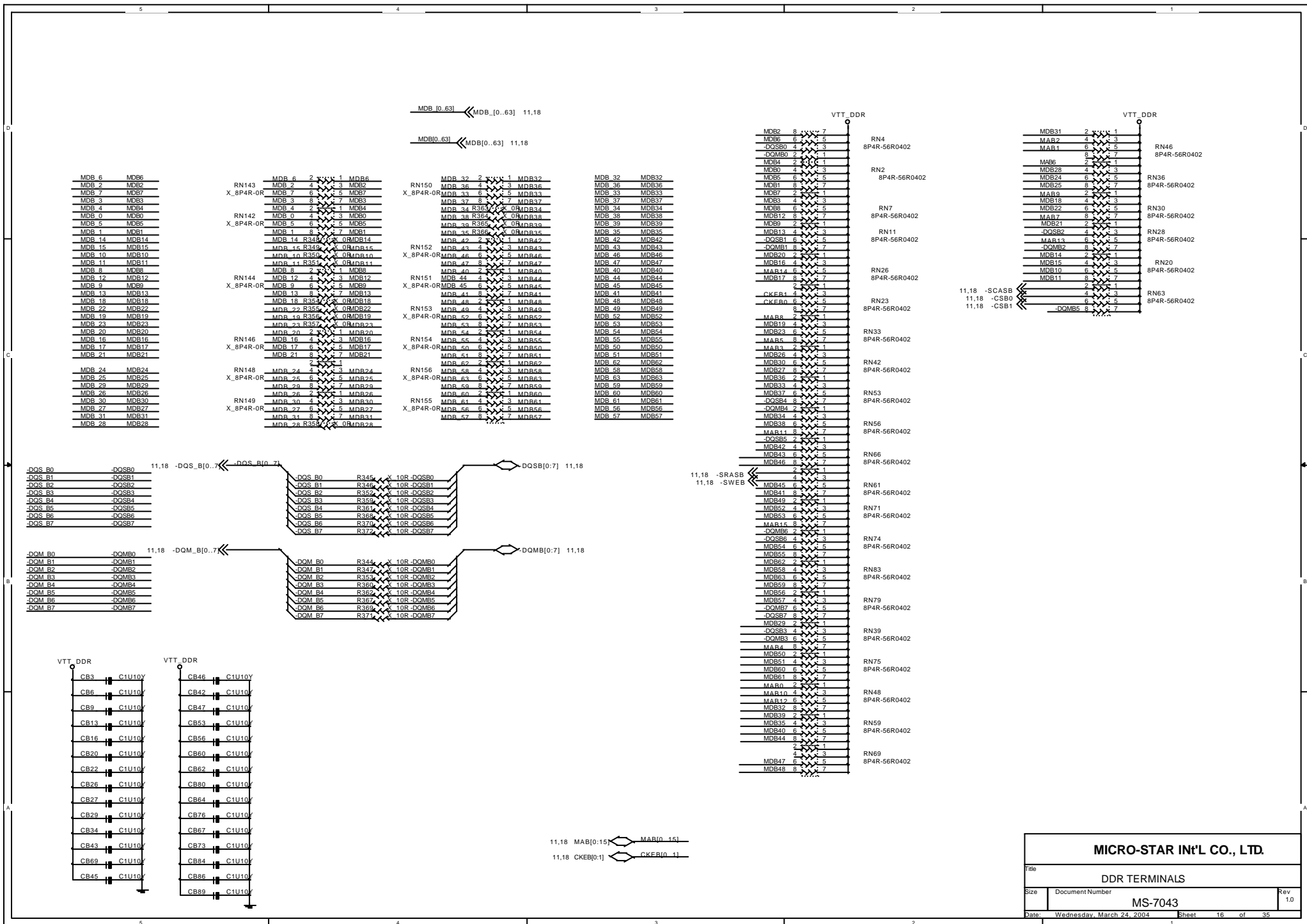
Monday, April 26, 2004

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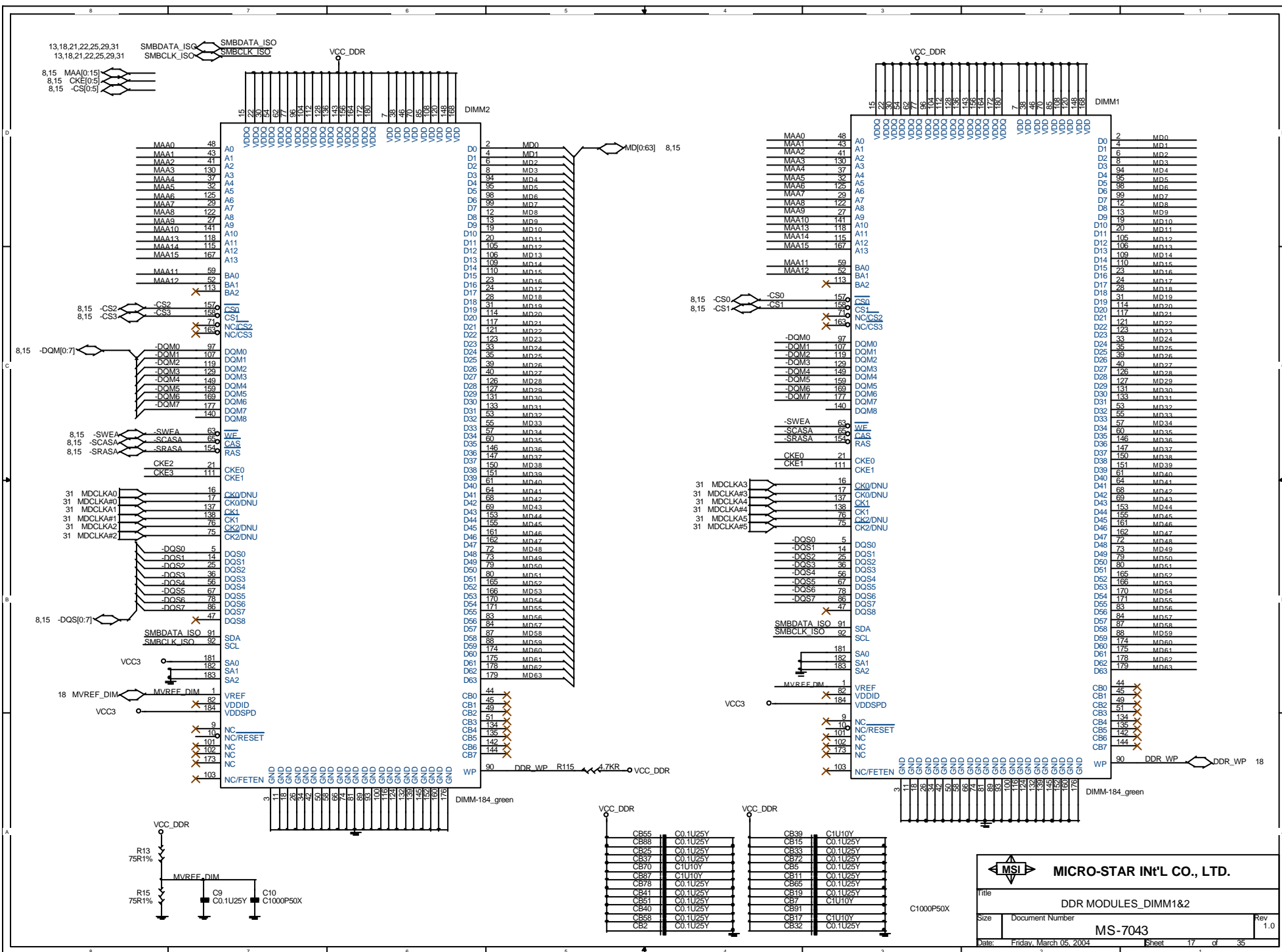
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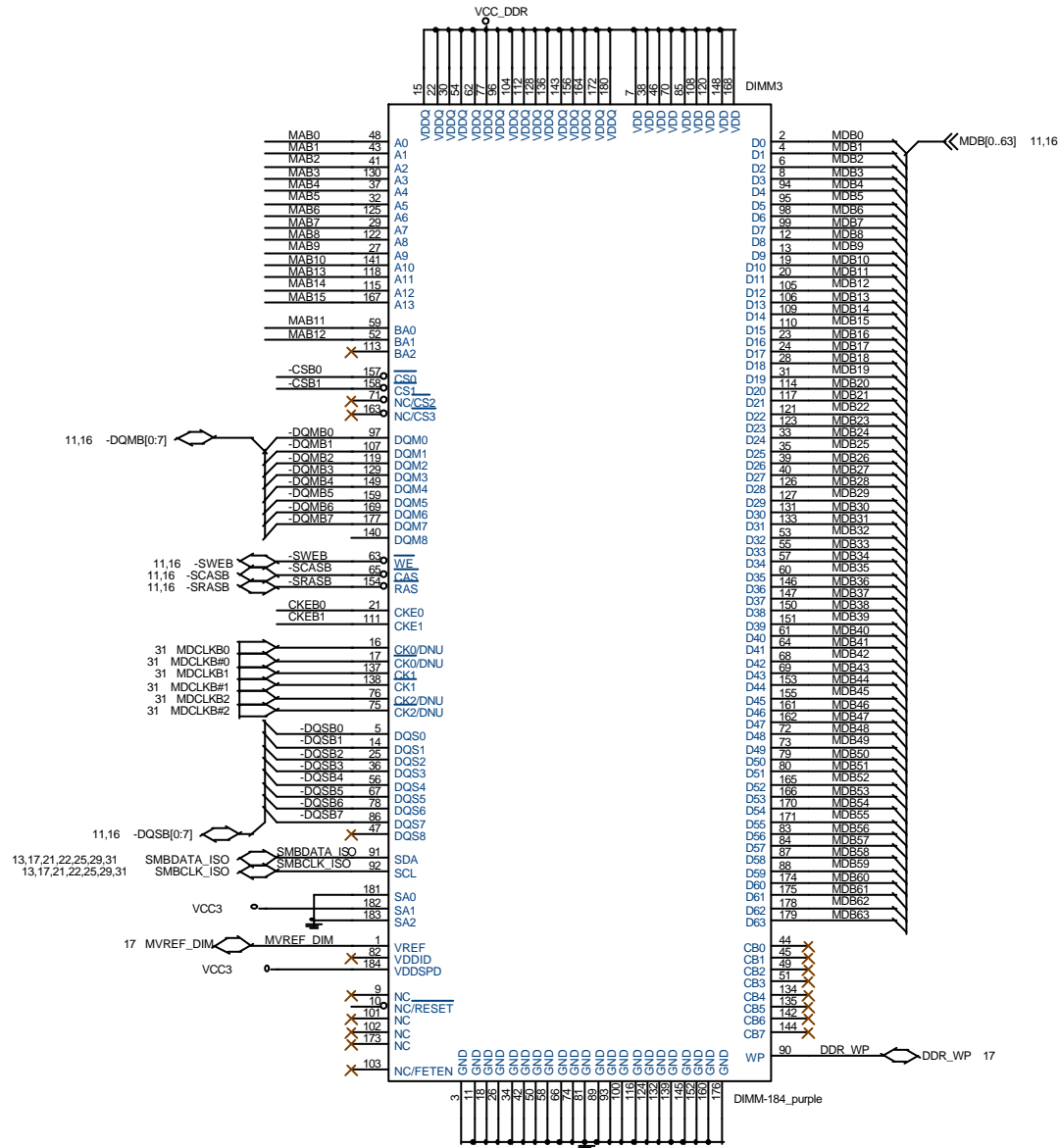
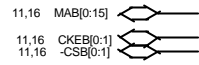




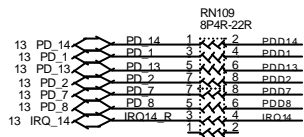
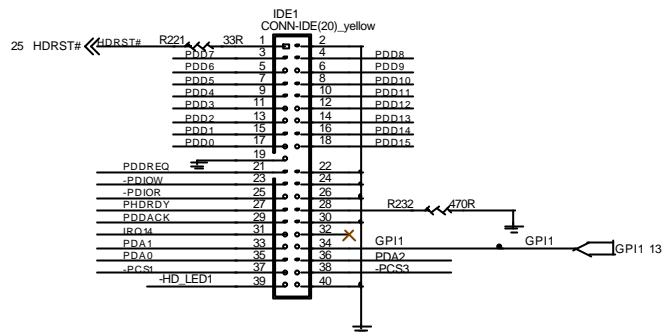




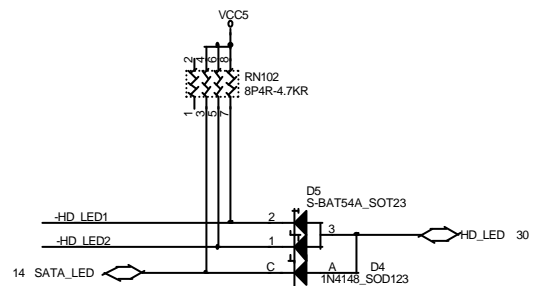
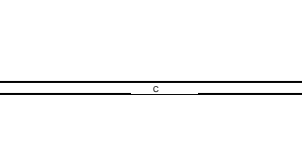
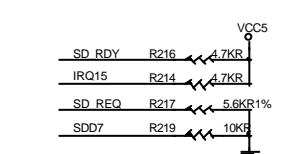
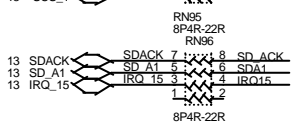
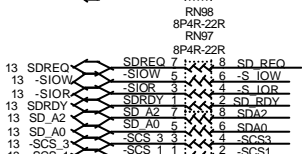
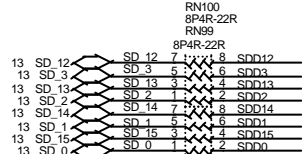
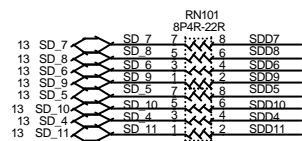
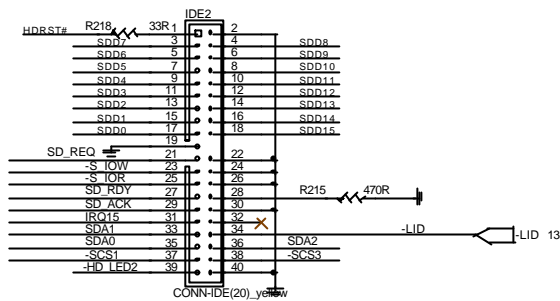




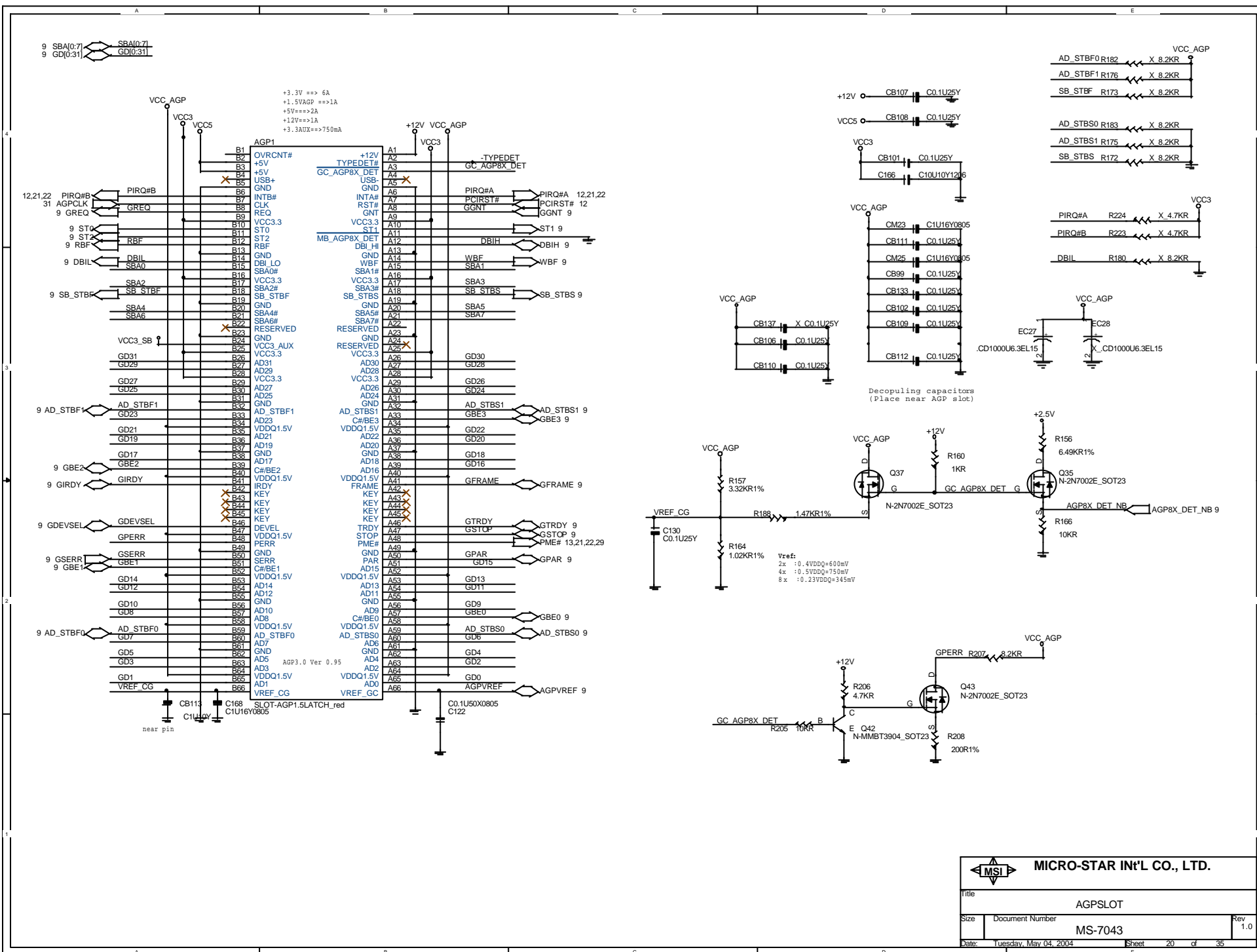
# PRIMARY



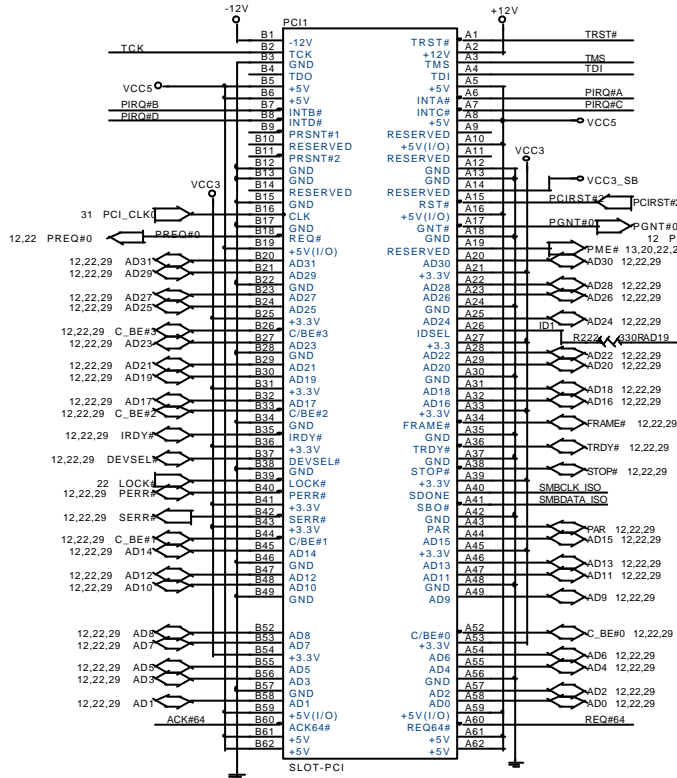
# SECONDARY



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Title IDE CONNECTORS			
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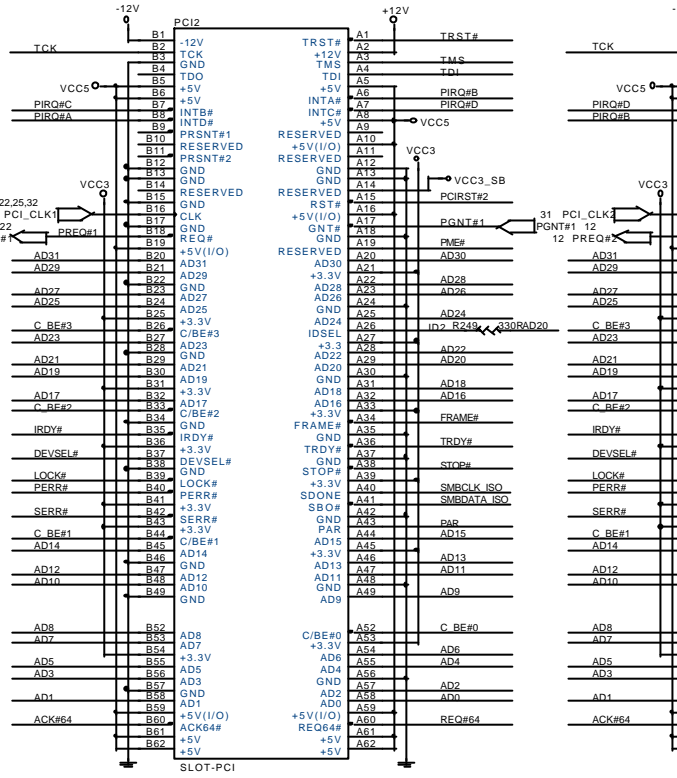


# PCI SLOT1(PCIVER:2.2COMPLY)



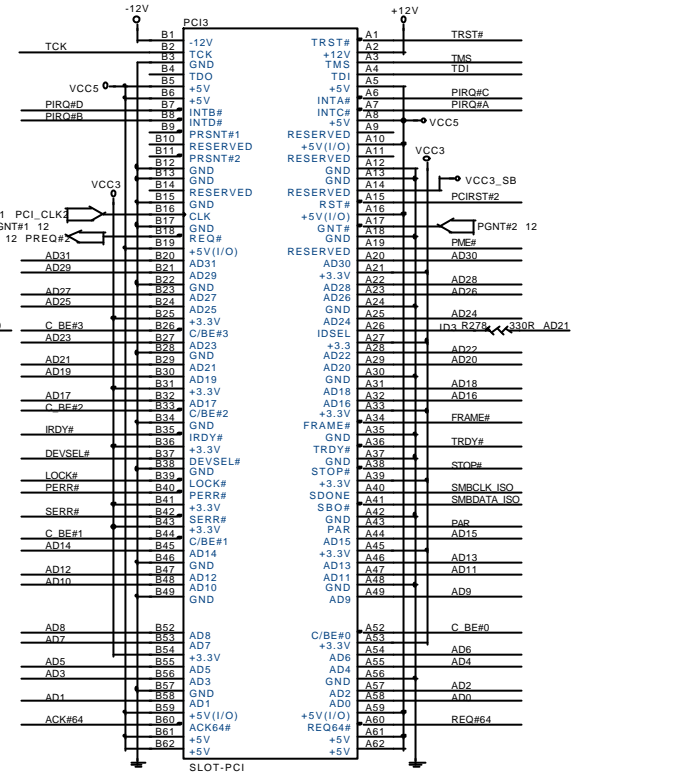
**IDSEL = AD19**  
**MASTER = PIRQ#5**  
**PIRQ#A**

# PCI SLOT2(PCIVER:2.2COMPLY)



**IDSEL = AD20**  
**MASTER = PIRQ#1**  
**PIRQ#B**

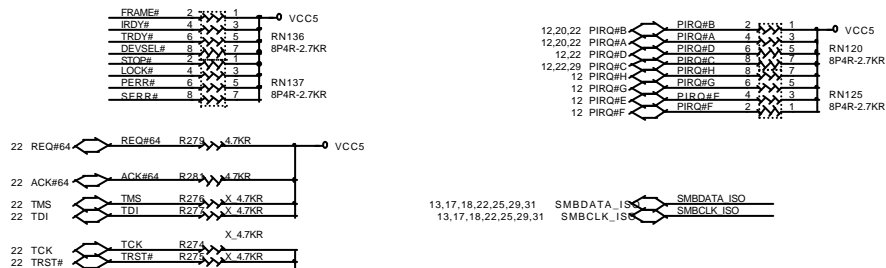
# PCI SLOT3(PCIVER:2.2COMPLY)



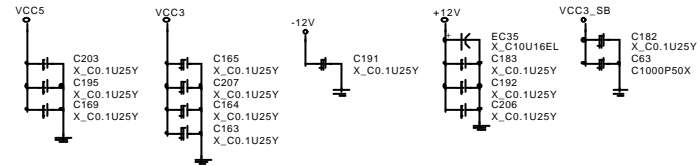
**IDSEL = AD21**  
**MASTER = PIRQ#2**  
**PIRQ#C**

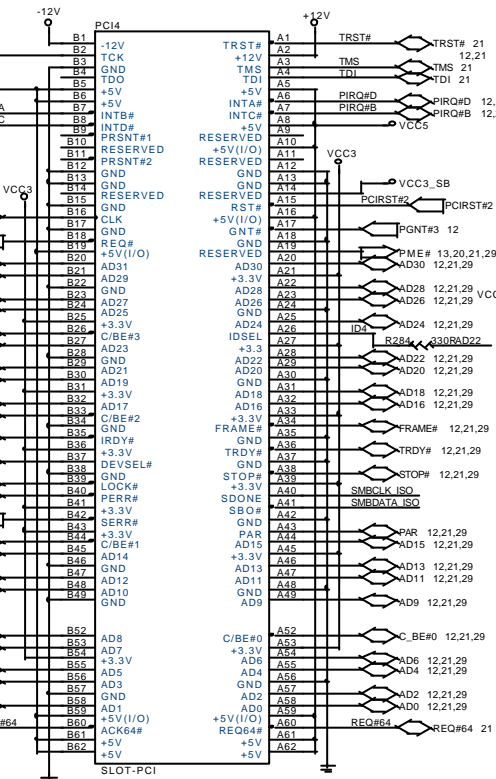
13,17,18,22,25,29,31 SMBCLK\_ISO  
13,17,18,22,25,29,31 SMBDATA\_ISO

## PCI PULL-UP /DOWNRESISTORS





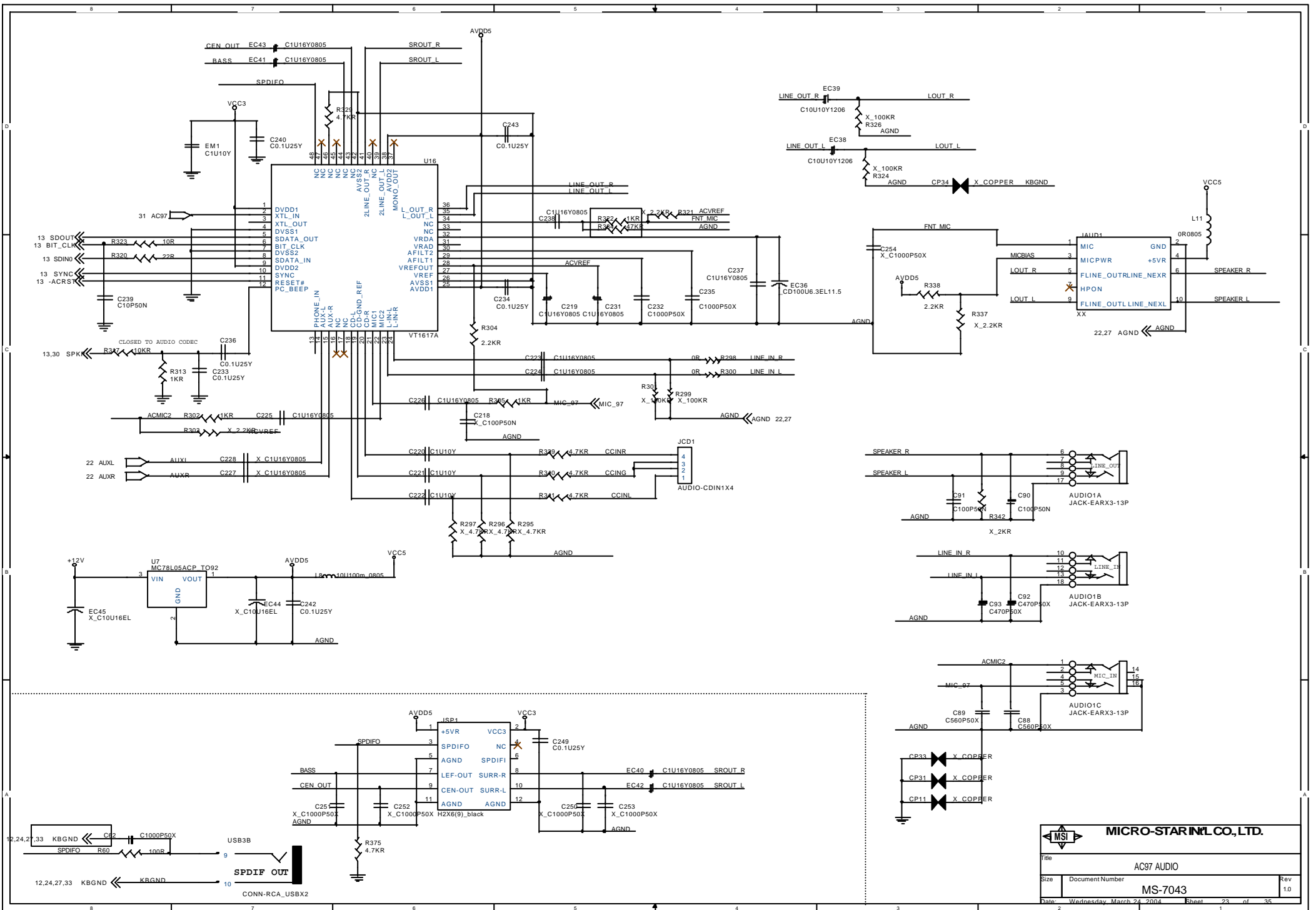
## PCI SLOT DECOUPLING CAPACITORS



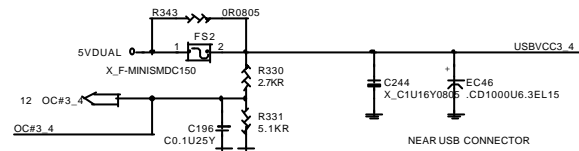


The diagram illustrates the pin configuration for a PCI Slot, showing the connection between the slot pins and the system components. The pins are organized into two main groups: the left side (pins 1-59) and the right side (pins 60-119). The left side pins are labeled with their functions, including TRST#, AGND, PIRQ#, INTA#, INTB#, INTO#, PRSNT#, PRSNT#2, GND, RESERVED, CLK, RST#, GNT#, BME#, AD#, DSE#, GND, AD#, TRDY#, DEVSEL#, LOCK#, PERR#, SERR#, C/BE#, AD#, GND. The right side pins are labeled with their functions, including AGND, PIRQ#A, PIRQ#B, VCC5, 33R, 5VDUAL, VCC3\_SB, PCIRST#2, PGNT#4, BME#, AD#, DSE#, GND, AD#, TRDY#, STOP#, SMBCLK ISO, SMBDATA ISO, PAR, AD#, C/BE#, GND, AD#, REQ#64, REQ#64. The diagram also shows the connection of the PCI Slot to the system power and ground planes.

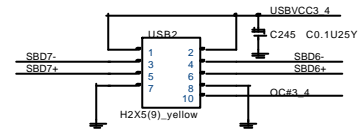
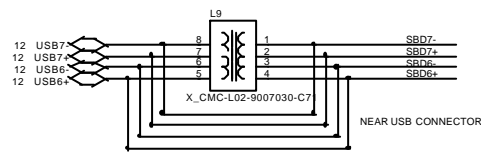
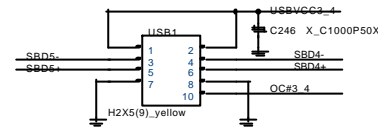
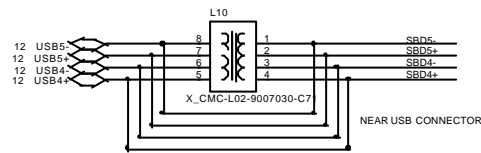
13,17,18,21,25,29,31	SMBCLK_ISO		SMBCLK ISO	R251		X 4.7KR
13,17,18,21,25,29,31	SMBDATA_ISO		SMBDATA ISO	R252		X 4.7KR



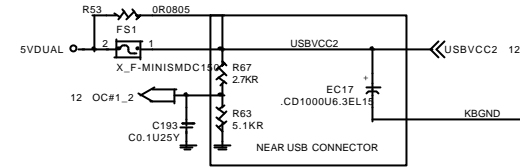
### POWER CIRCUIT FOR USB PORT 4,5,6,7



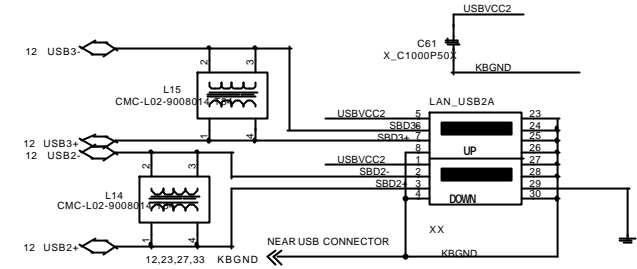
### REAR PANEL USB CONNECTOR FOR USB PORT 4,5,6,7



### POWER CIRCUIT FOR USB PORT 4,5

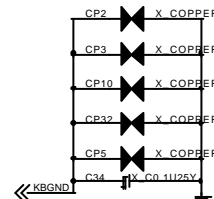
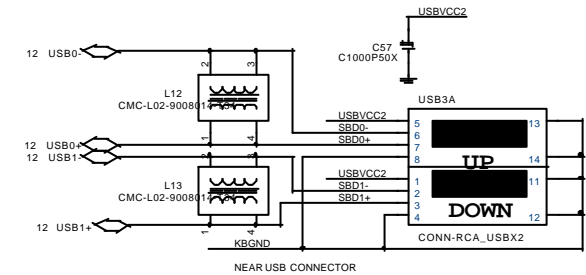


### REAR PANEL USB CONNECTOR FOR USB PORT 2,3



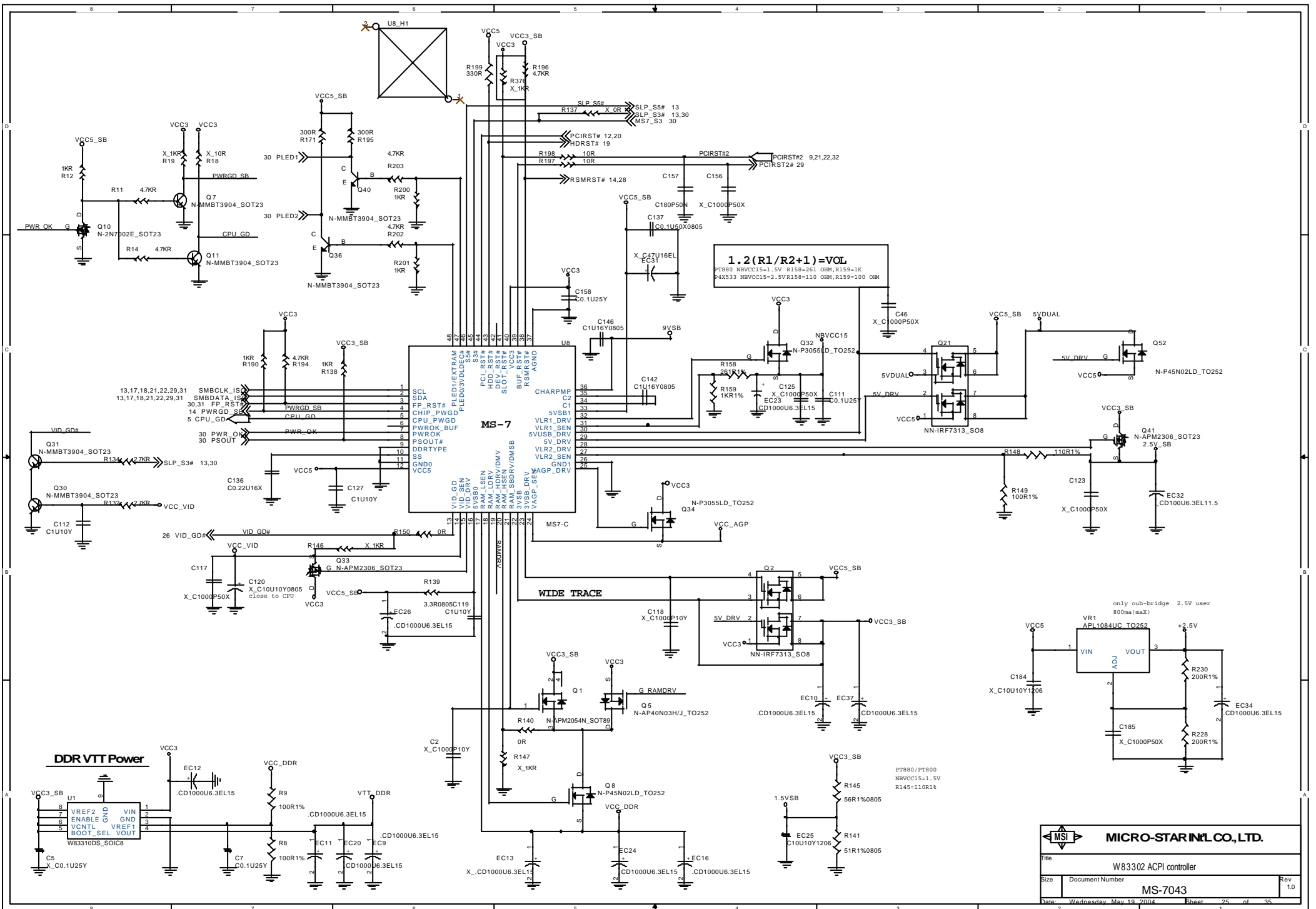
### POWER CIRCUIT FOR USB PORT 6,7

### REAR PANEL USB CONNECTOR FOR USB PORT 0,1

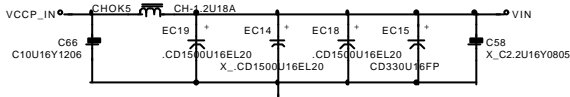


MSI MICRO-STAR INT'L CO., LTD.			
Title USB Connectors			
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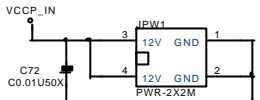




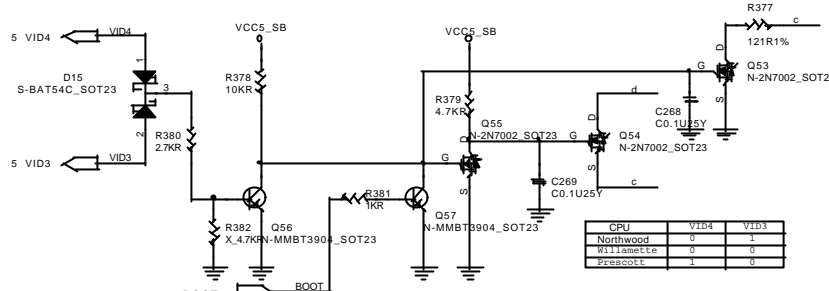
5 VID[0..5]  VID[0..5]



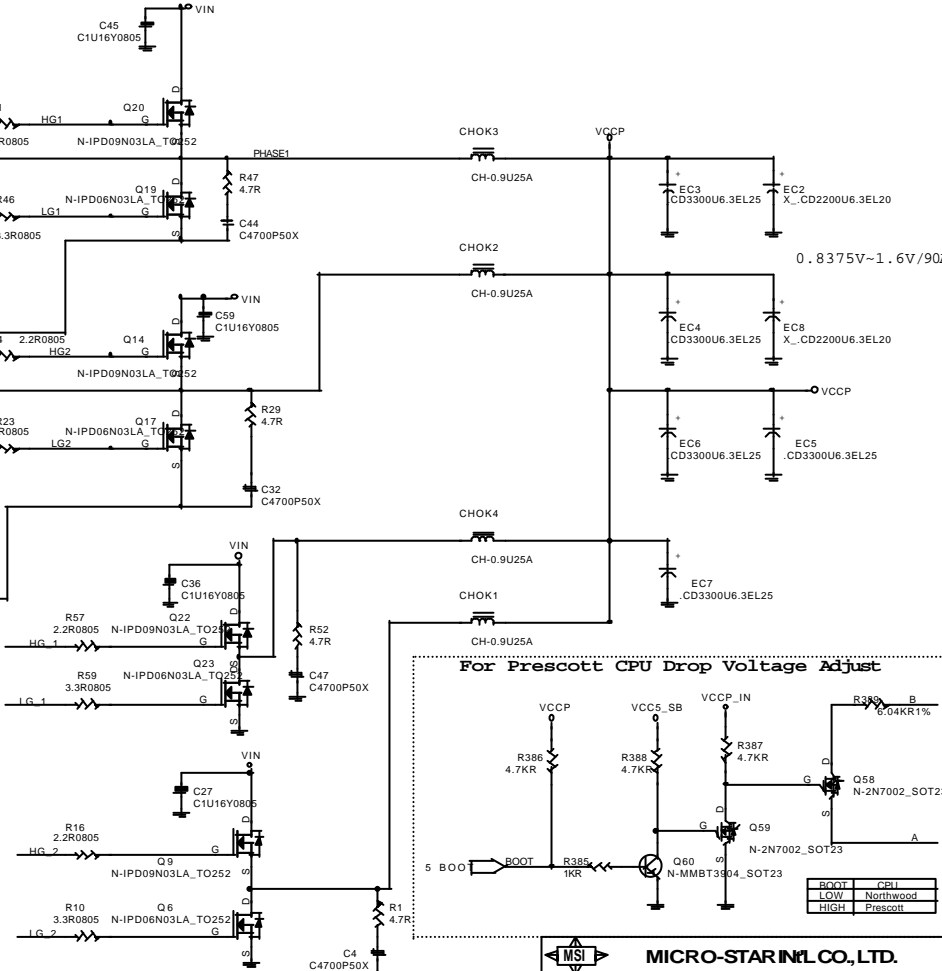
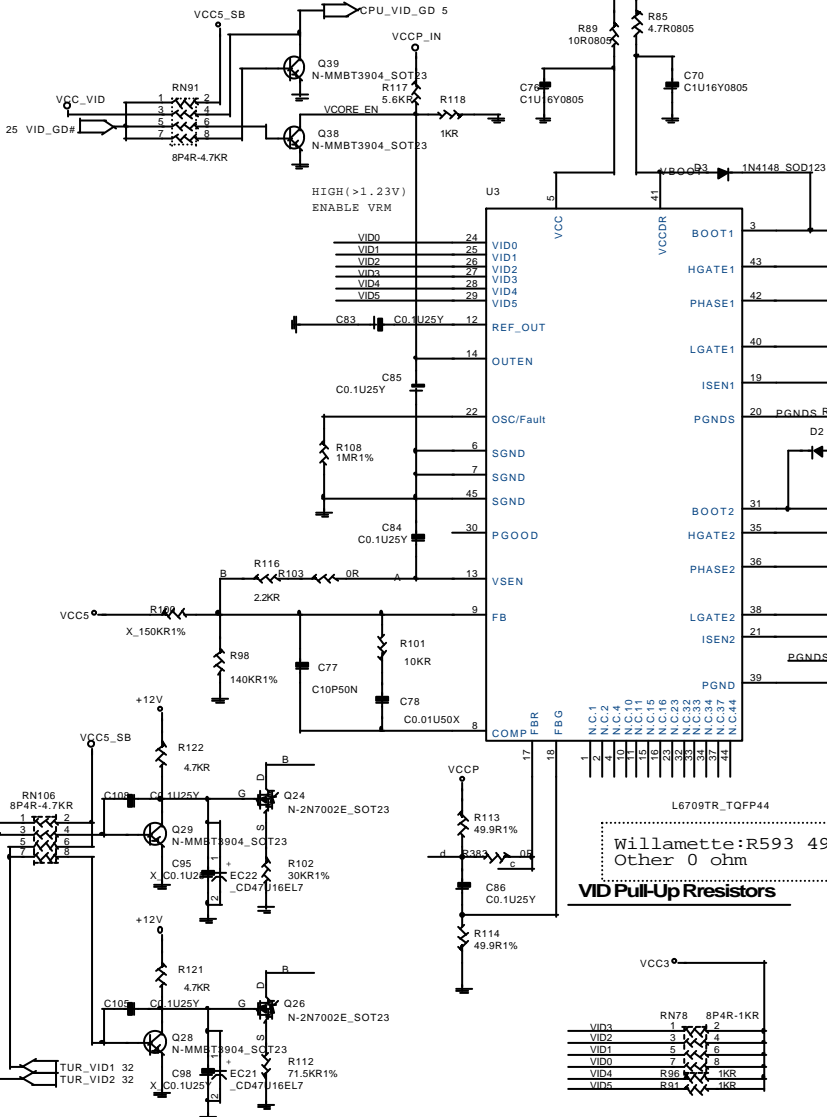
### ATX12V Power Connector



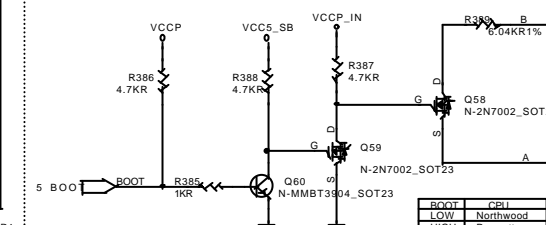
### For Willamette CPU Offset Voltage Adjust



CPU	VID4	VID3
Northwood	0	1
Willamette	0	0
Prescott	1	0



## For Prescott CPU Drop Voltage Adjust

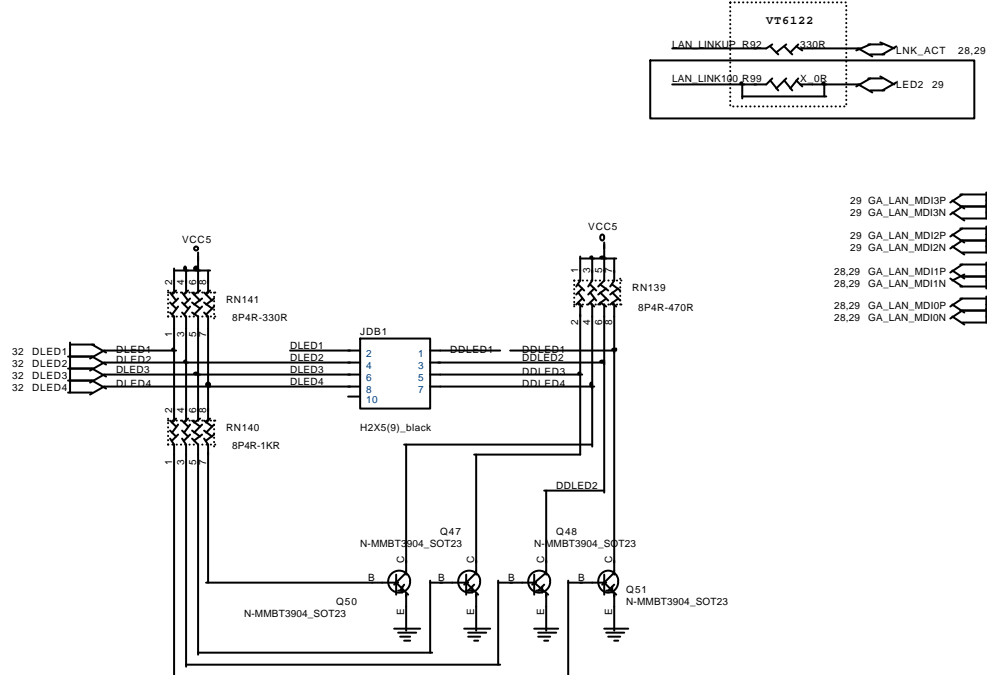


BOOT	CPI
LOW	Northwood
HIGH	Prescott



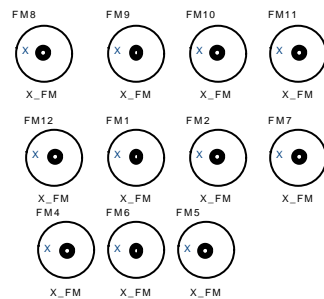
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Title		VRM 10	
Size	Document Number	Rev	
	MS-7043	1.	
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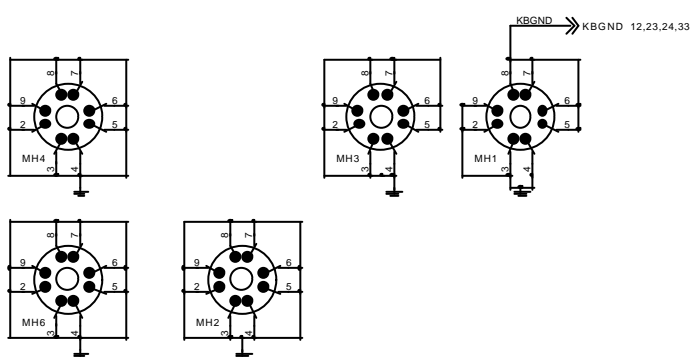


	6103L	6122
R93	0 OHM	X
R72	0 OHM	0 OHM
R88	330 OHM	X
R87	X	330 OHM
R94	330 OHM	X
R97	0 OHM	X
R99	X	X
R92	X	330 OHM
c75	0.10	X
c64	0.10	X
R73	X	0 OHM

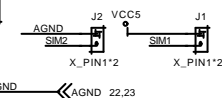
### Optics Orientation Holes

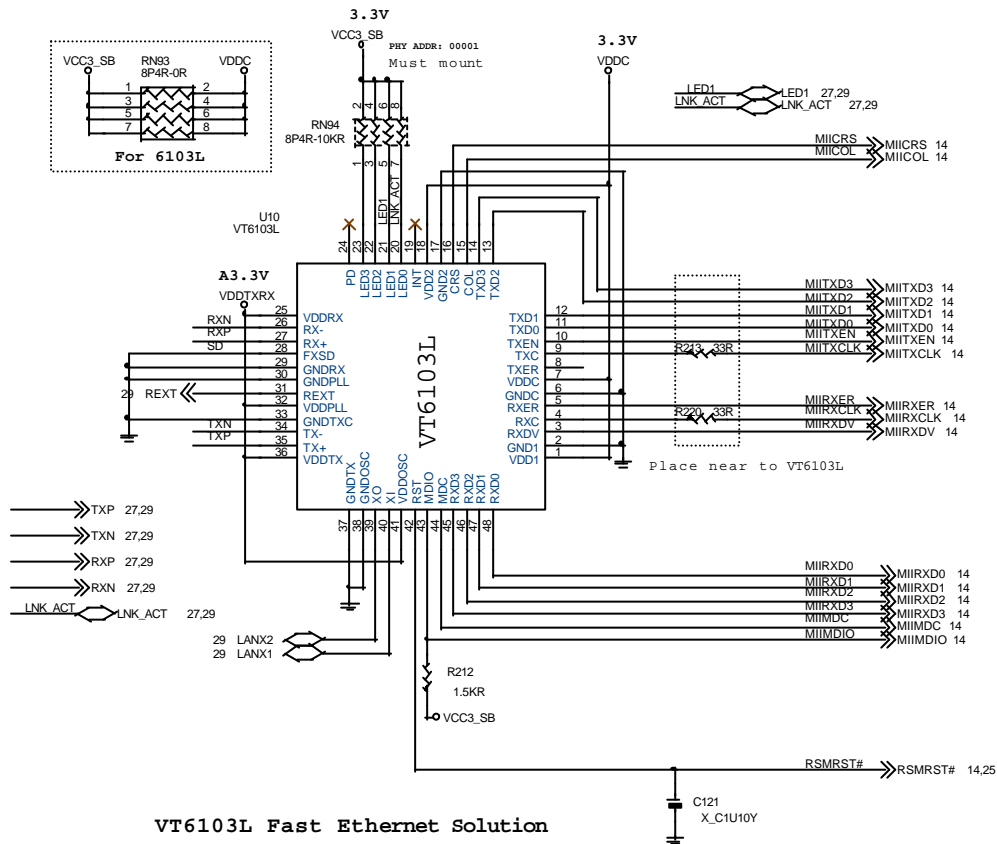


### Mounting Holes



### Simulation





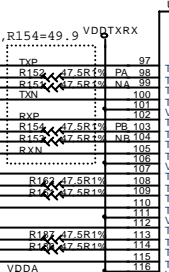
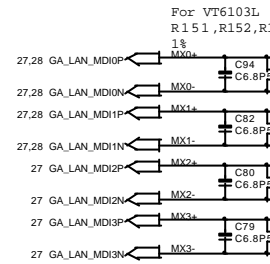
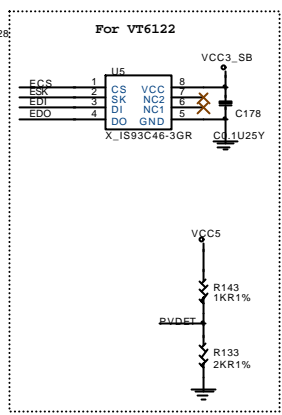
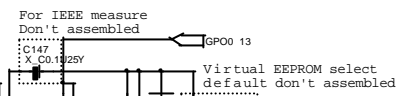
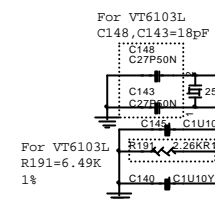
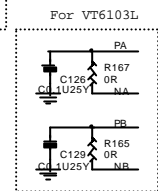
#### Change Part

Capacitor	C1=C2=18pF
Resistor	R8=6.49K 1% R10=R12=R13=R15=49.9 1%
Other	CN1=P35-152-1GP9

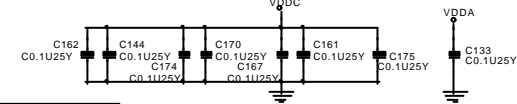
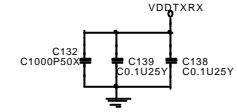
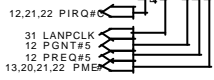
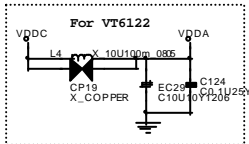
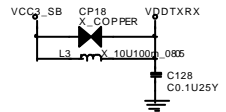
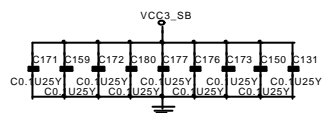
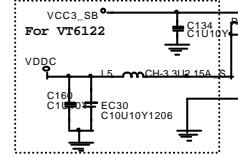
#### Remove Part value

Capacitor	C3, C4, C10, C22, C28, C29, C31, C40, C45
Resistor	R1, R2, R3, R4, R16, R17, R18, R19, R22, R23
Other	FB2, L1, U1, U2

USB-RJ45-LED-P35-152-1GJ9(Speed Tech) for VT6122  
 USB-RJ45-LED-P35-152-1GP9(Speed Tech) for VT6103L



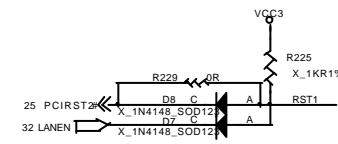
VT6122  
 GIGA NIC  
 LQFP-128



### VT6122 Gigabit Ethernet Solution

#### Remove Part

Capacitor	C4, C12, C15, C16, C24
Resistor	RN1, R11, R14, R24, R25, R27, R30, R32, R35
Other	U5



**MICRO-STAR INT'L CO., LTD.**

Title: VT6122 Gigabit Ethernet

Size: Document Number

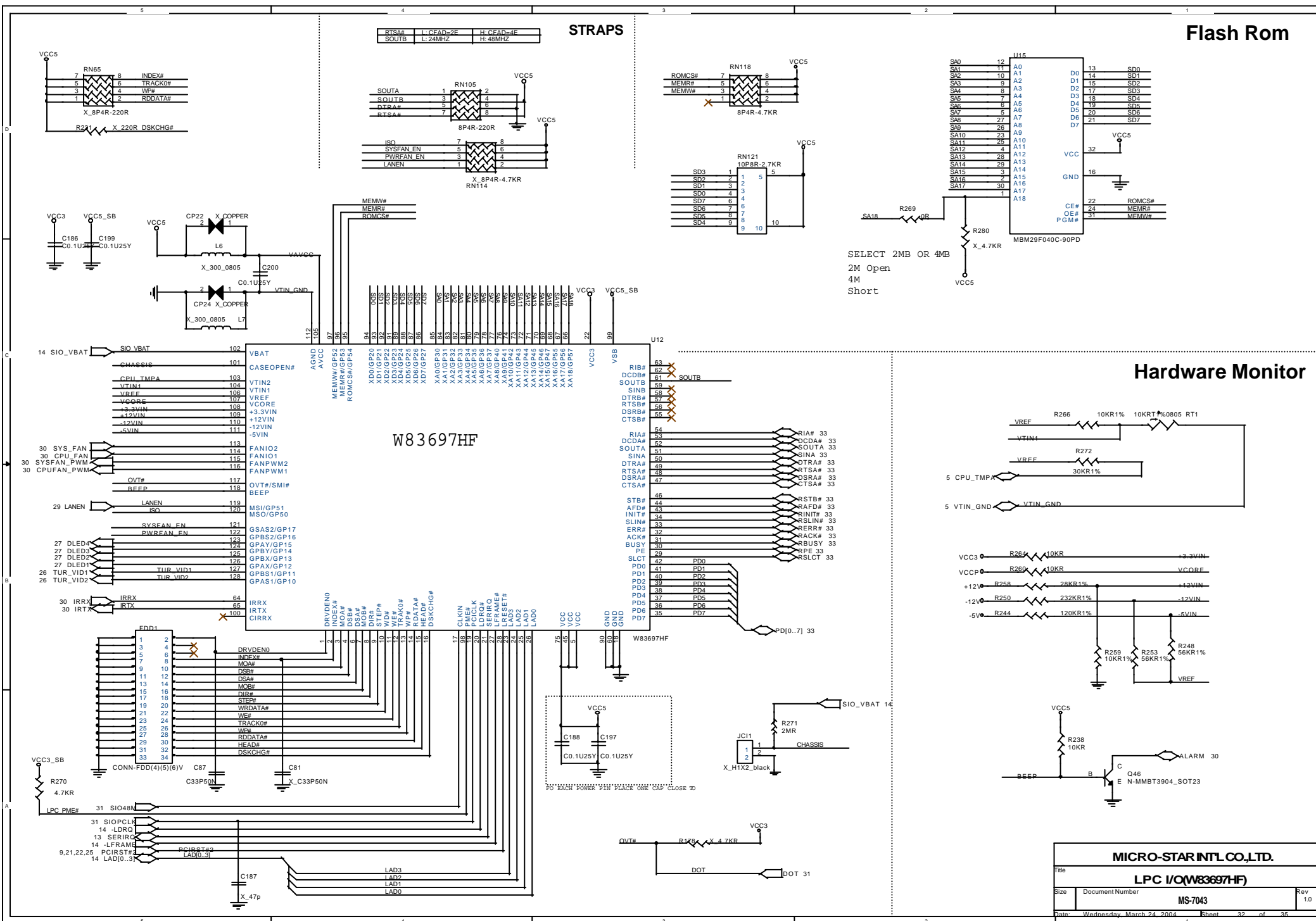
MS-7043

Date: Wednesday, March 24, 2004 Sheet: 29 of 35

## AT2

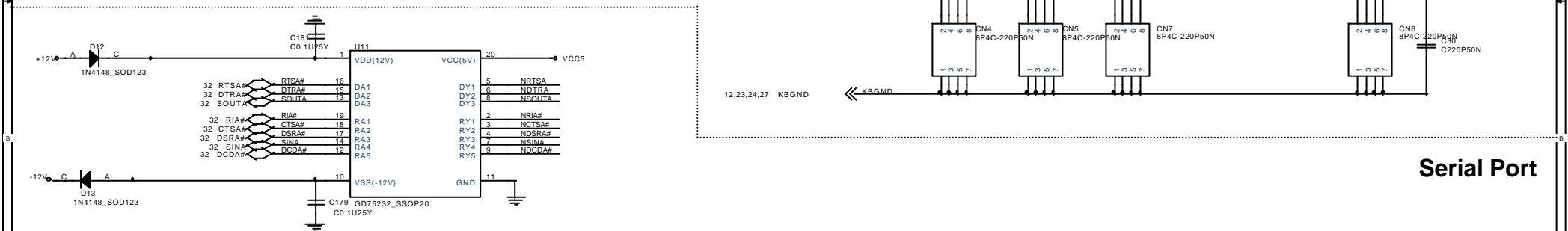
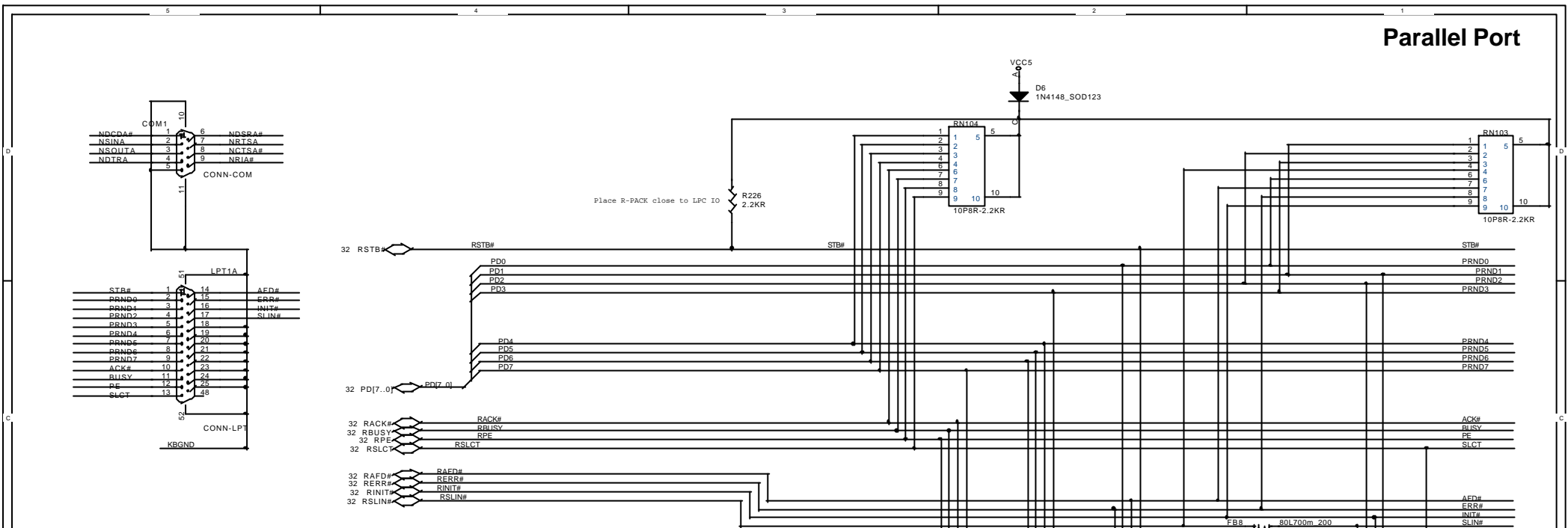








## Parallel Port



## Serial Port

